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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/695,453 | 10/29/2003 | Ippei Fujimoto | T36-159874M/KOH | 4570 |

21254 7590 03/31/2006

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| EXAMINER | |
|---|---|
| WILLIAMS, ALEXANDER O | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 03/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/695,453 | FUJIMOTO ET AL. | |
| | Examiner | Art Unit | |
| | Alexander O. Williams | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3 and 7-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-23* is/are allowed.

6)☒ Claim(s) *1 and 3* is/are rejected.

7)☒ Claim(s) *2 and 7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/695453 Attorney's Docket #: T36-159874M/RS
Filing Date: 10/29/03; claimed foreign priority to 10/31/02

Applicant: Fujimoto et al.

Examiner: Alexander Williams

This action being remailed to indicated that the last office action was suppose to be non-final. Time will be restarted as of the mailing of this office action.

Applicant's RCE filed 11/10/05 has been acknowledged.

Applicant's Request for Reconsideration and Applicant initiated interview request prior to the first office action after the filing of an RCE filed 11/10/05 in the election of species corresponding to figure 1 (claims 1 to 3), filed 9/30/2004, has been acknowledged.

Claims 4-6 have been canceled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

**Initially, it is noted that the 35 U.S.C. § 103 rejection based on an electrode and a polycrystalline metal comprising a transition metal deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.**

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claim 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nomoto (U.S. Patent # 6,320,216 B1).

1. For example, Nomoto (figures 1 to 11B) specifically figure 1 show an electrode **7,4d,6,4c,5b,5b,5a** for p-type Group III nitride compound semiconductor layer **4a**, comprising a film at least containing polycrystalline metal **6**, wherein said polycrystalline metal comprises a transition metal **5b,5a (see column 10, lines 27-37)**.

4) FIG. 1 is a top view of the structure of a memory device according to a first embodiment of the present invention. FIG. 2 shows the section structure of the memory device of FIG. 1 taken along a line I--I of FIG. 1. In this memory device, a source electrode 2 and a drain electrode 3 each made of suitable metal are formed on a suitable substrate 1 having an interval in between. On the top of the substrate 1 between the source electrode 2 and the drain electrode 3, a charge accumulation layer 6 and a barrier layer 4d are stacked via a plurality of barrier layers serving as barrier portions and one or more transition layers each formed between barrier layers (here, three barrier layers 4a, 4b and 4c, and two transition layers 5a and 5b formed in between). Thereon, a gate electrode (control electrode) 7 made of suitable metal is formed. The gate electrode 7 and the barrier layer 4d are in a non-ohmic junction state.

(5) On the surface of the substrate 1 between the source electrode 2 and the drain electrode 3, two-dimensional electron gas (2DEG) is accumulated and a conduction layer 1a serving as a current passage is formed. The conduction layer 1a is in an ohmic junction state with source electrode 2 and the drain electrode 3 respectively. On the surface of the substrate 1, a device isolation portion 8 for isolating this memory device from other devices is formed so as to surround a predetermined region located between the source electrode 2 and the drain electrode 3.

(6) At least the surface (the surface on which the source electrode 2 and so on are formed) of the substrate 1 is made of a suitable semiconductor. For example, a semiconductor substrate made of a suitable semiconductor may be used as the substrate 1. It is also possible to use a substrate obtained by forming a suitable semiconductor thin film on a surface of a substrate main body made of sapphire or suitable glass or plastic, such as a SOI (Silicon-On-Insulator) substrate or a SOS (Silicon-On-Sapphire) substrate. In other words, the conduction layer 1a is made of a suitable semiconductor. Furthermore, the barrier layers 4a, 4b, 4c and 4d, the transition layers 5a and 5b, and the charge accumulation layer 6 are also made of suitable semiconductors respectively.

(7) However, the barrier layer 4a formed between the conduction layer 1a and the transition layer 5a is made of a semiconductor which has a smaller electron affinity or a larger work function

than the semiconductor forming the conduction layer 1a (i.e., the substrate 1) and the semiconductor forming the transition layer 5a. Also, the barrier layer 4b formed between the transition layers 5a and 5b is made of a semiconductor which has a smaller electron affinity or a larger work function than the semiconductor forming the transition layer 5a and the semiconductor forming the transition layer 5b. Furthermore, the barrier layer 4c formed between the transition layer 5b and the charge accumulation layer 6 is made of a semiconductor which has a smaller electron affinity or a larger work function than the semiconductor forming the transition layer 5b and the semiconductor forming the charge accumulation layer 6. In addition, the barrier layer 4d formed between the charge accumulation layer 6 and the gate electrode 7 is made of a semiconductor which has a smaller electron affinity or a larger work function than the semiconductor forming the charge accumulation layer 6.

(8) For example, the conduction layer 1a, the transition layers 5a and 5b, and the charge accumulation layer 6 are made of Si (silicon), and the barrier layers 4a, 4b, 4c and 4d are made of SiO.sub.2, Si.sub.3 N.sub.4 (silicon nitride) or SiON. Alternatively the conduction layer 1a, the transition layers 5a and 5b, and the charge accumulation layer 6 are made of SiGe or Ge (germanium), and the barrier layers 4a, 4b, 4c and 4d are made of SiGe, Si, SiO.sub.2, Si.sub.3 N.sub.4 or SiON respectively. Or the conduction layer 1a, the transition layers 5a and 5b, and the charge accumulation layer 6 are respectively made of a Group III-V compound semiconductor including at least one element selected from the group consisting of In (indium) and Ga (gallium) of Group III element and As (arsenic) of the Group V element, and the barrier layers 4a, 4b, 4c and 4d are made of a Group III-V compound semiconductor including at least one element selected from the group consisting of In, Al (aluminum) and Ga of the Group III element and As of the Group V element. Alternatively, the conduction layer 1a, the transition layers 5a and 5b, and the charge accumulation layer 6 are made of a Group III-V compound semiconductor including at least one element selected from the group consisting of In and Ga of the Group III element and Sb (antimony) of the Group V element, and the barrier layers 4a, 4b, 4c and 4d are respectively made of a Group III-V compound semiconductor including at least one element selected from the group consisting of In, Al and Ga of the Group III element and Sb of the Group V element.

(25) Such a memory device can be fabricated as described below. It is now assumed that a single crystal Si substrate is used as the substrate 1 and the barrier layers 4a, 4b, 4c and 4d are respectively made of SiO.sub.2. It is further assumed that the transition layers 5a and 5b and the charge accumulation layer 6 are made of polycrystal Si and each of the source electrode 2, the drain electrode 3 and the gate electrode 7 are made of Al respectively. The fabrication method in this case will now be described specifically.

(48) Here, the barrier layers 4a, 4b, 4c and 4d are made of a suitable insulator, and the **transition layers 5a and 5b,** and the charge accumulation layer 6 are made of suitable metal respectively. For example, the conduction layer 1a is made of **Si,** the **barrier layers 4a, 4b, 4c and 4d are made** of **Al.sub.2 O.sub.3 (aluminum oxide),** and the transition layers 5a and 5b, and the charge accumulation layer 6 are made of Al respectively. Furthermore, **the barrier layers 4a, 4b, 4c and 4d may be made of an insulator such as TiOx or NbOx, and the transition layers 5a and 5b may be made of metal such as Ti or Nb respectively.**

Therefore, it would have been obvious to one of ordinary skill in the art to use the electrode and a polycrystalline metal comprising a transition metal as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 2 and 7-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 11-23 are allowed.

# Response

Applicant's arguments filed 11/10/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above and in the interview summary in discussing why the outstanding rejection remain applied.

| Field of Search | Date |
|---|---|
| U.S. Class and subclass:<br>257/744,745,123,94,103,627,82,85,90,96,336,77,628,341,335,14,98,103,190<br>257/64,103,60,65,66,37,78,37;40,50,51,96,82,85,744,745,347,184,94,95 | 10/3/04<br>5/13/05<br><br>8/9/05<br>1/19/06 |
| Other Documentation:<br>foreign patents and literature in<br>257/744,745,123,94,103,627,82,85,90,96,336,77,628,341,335,14,98,103,190<br>257/64,103,60,65,66,37,78,37,40,50,51,96,82,85,744,745,347,184,94,95 | 10/3/04<br>5/13/05<br><br><br>8/9/05<br>1/19/06 |
| Electronic data base(s):<br>U.S. Patents EAST | 10/3/04<br>5/13/05<br>8/9/05<br>1/19/06 |

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30 AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
1/19/06

Alexander O Williams
Primary Examiner
Art Unit 2826